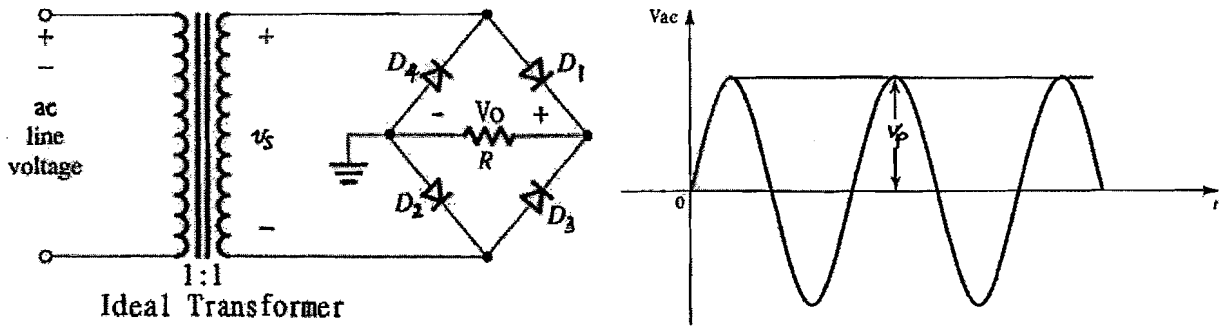
中國文化大學 99 學年度碩士班考試入學招生考試

系所組：機械工程學系數位機電碩士班丙組

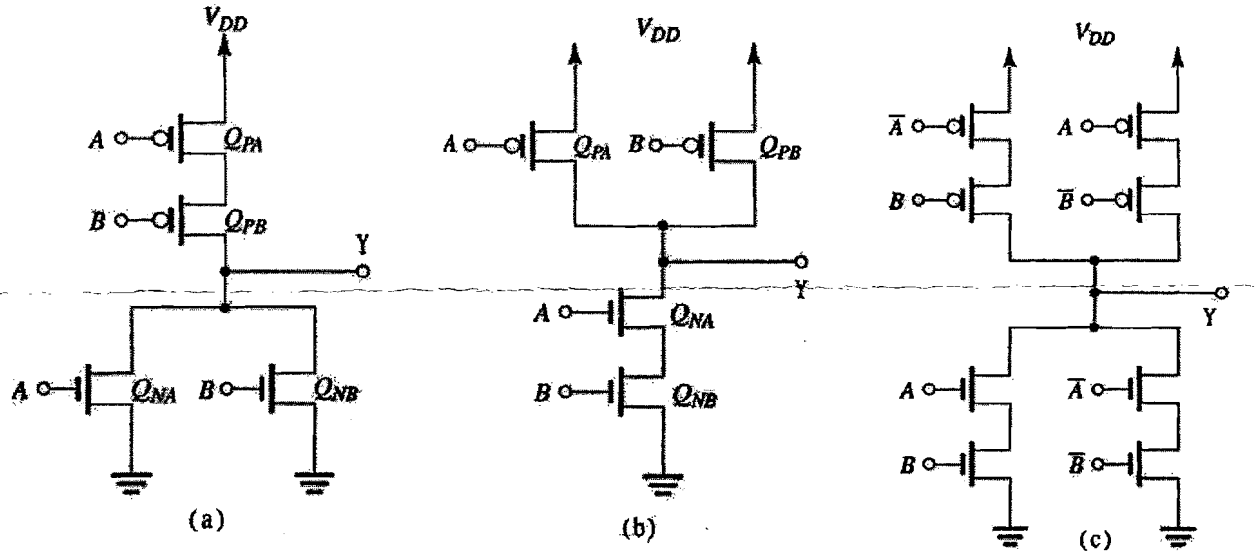
日期節次：99 年 3 月 13 日第 2 節 11:00 -12:30

科目：電子學

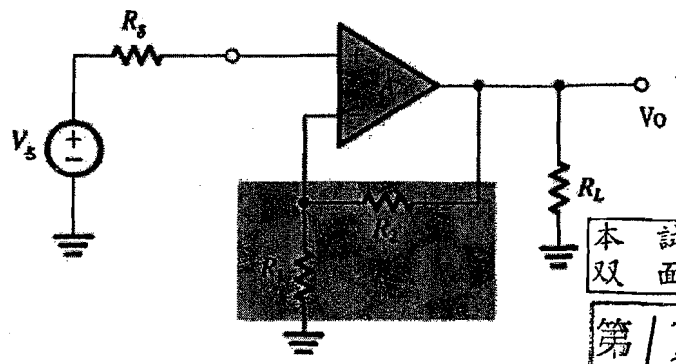
1. Give a Bridge Rectifier, shown at the left part of the following figure. A sinusoidal input voltage source, v_{ac}, is an AC voltage source with its peak equal to V_p. The waveform of v_{ac} is drawn at the right part of the given figure. It has assumed that all diodes are ideal diodes. Please plot the waveform of output voltage, V_o, with respect to input voltage source. [15]



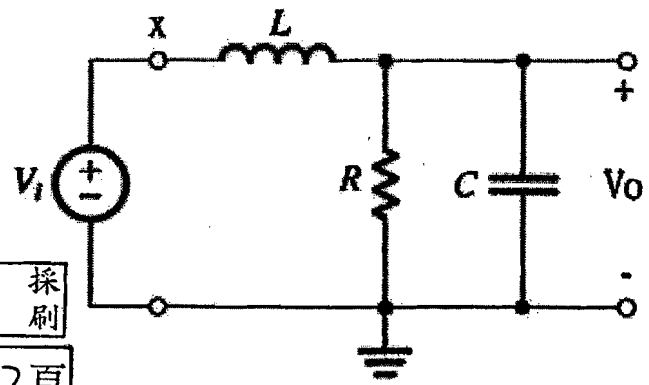
2. Give three CMOS circuits, shown as follows. Please write down the digital operations of output Y. [15]



3. A non-negative OP-AMP circuit with an implementation of a feedback loop is shown on the following figure. It has assumed that the OP-AMP has infinite input and zero output resistance. Please answer these questions: (a) Find out the expression of the feedback factor, β. (b) If the open-loop voltage gain of this OP-AMP is 10^4 ($A=10^4$), find out R_2/R_1 to obtain a closed-loop voltage gain A_f of 10. [15]



4. Give a RLC circuit, shown as follow figure. [15]
   (a) Please derive the transfer function, T(s), where s=jw.
   (b) Please determine what type filter operation it is.
   (c) Give a brief explanation of the previous question and find out the natural frequency (w_0) and quality factor (Q).



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第 1 頁共 2 頁

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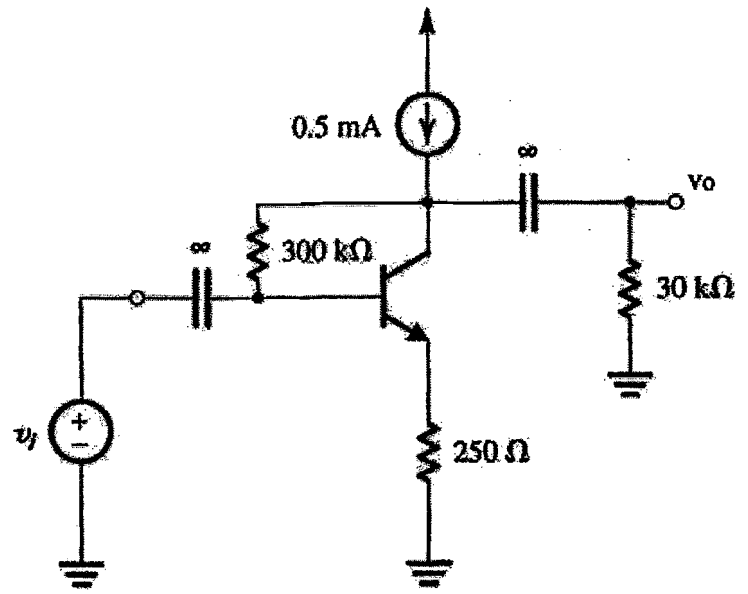
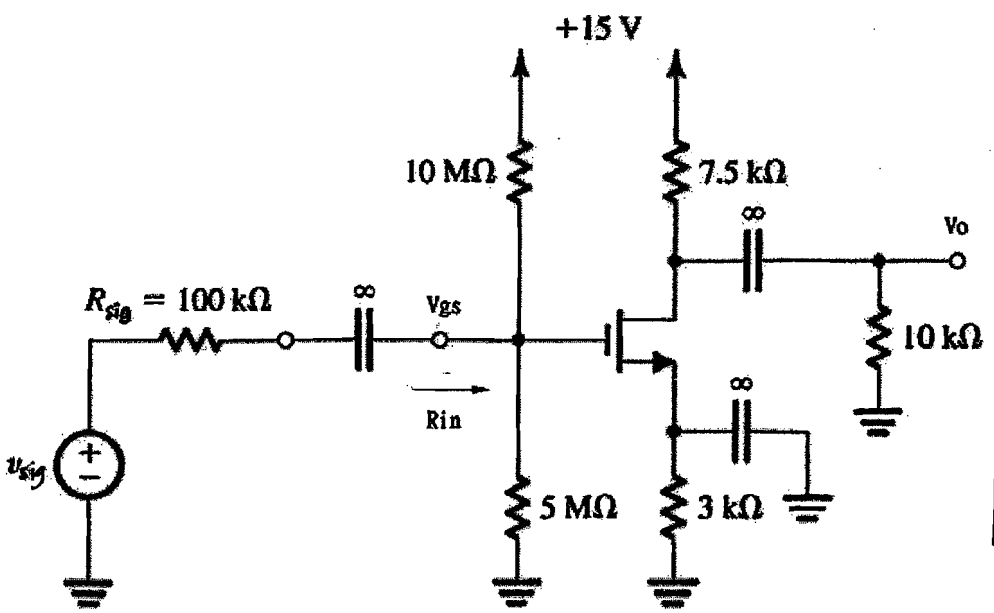
5. A circuit containing a BJT is shown on the following figure, which the β is equal to 100. [20]
   (a) Find the dc collector current and dc voltage at the collector.
   (b) Replacing the transistor by its T model, draw the small signal equivalent circuit of the amplifier. Analyze the resulting circuit to determine the voltage gain v_O/v_i.



6. A discrete CS amplifier circuit is employing the classical biasing scheme. The input signal v_{sig} is coupled to the gate through a very large capacitor (shown as infinite). The transistor source is connected to ground at signal frequencies via a very large capacitor (shown as infinite). The output voltage signal that develops at the drain is coupled to a load resistance via a very capacitor (shown as infinite). [20]
   (a) If the transistor has V_t=1V, and k_n' W/L=2mA/V^2, verify that the bias circuit establishes V_{GS} = 2V, I_D=1 mA, and V_D=+7.5 V. That is, assume these values, and verify that they are consistent with the values of the circuit components and the device parameters.
   (b) Find g_m and r_o if V_A = 100 V.
   (c) Draw a complete small-signal equivalent circuit for the amplifier assuming all capacitors behave as short circuits at signal frequencies.
   (d) Find R_{in}, v_{gs}/v_{sig}, v_o/v_{gs}, and v_o/v_{sig}.



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